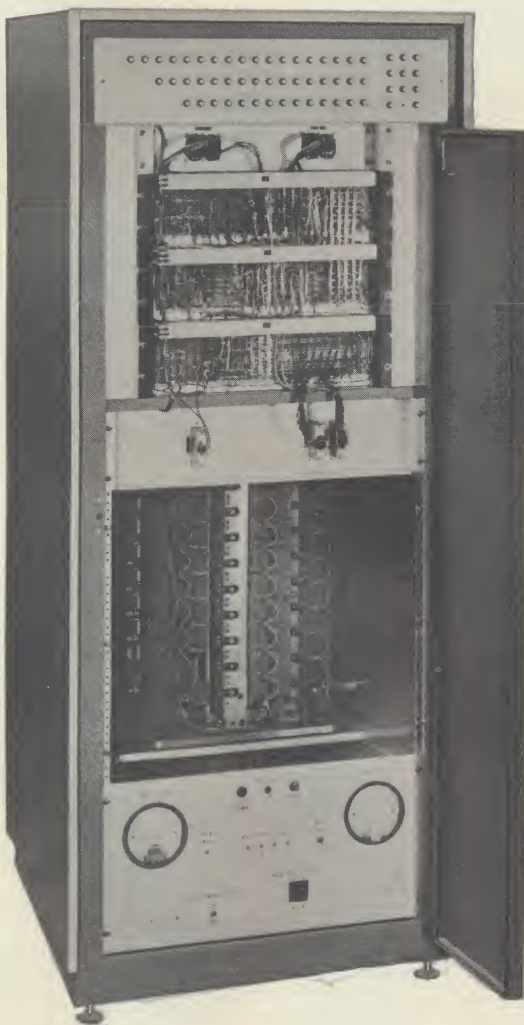


Vermont Research
CORPORATION

Precision Park • North Springfield, Vermont 05150 • 802/886-2256

DRUM MEMORIES MODULES • SYSTEMS

Drum Memory System *Model 1116*



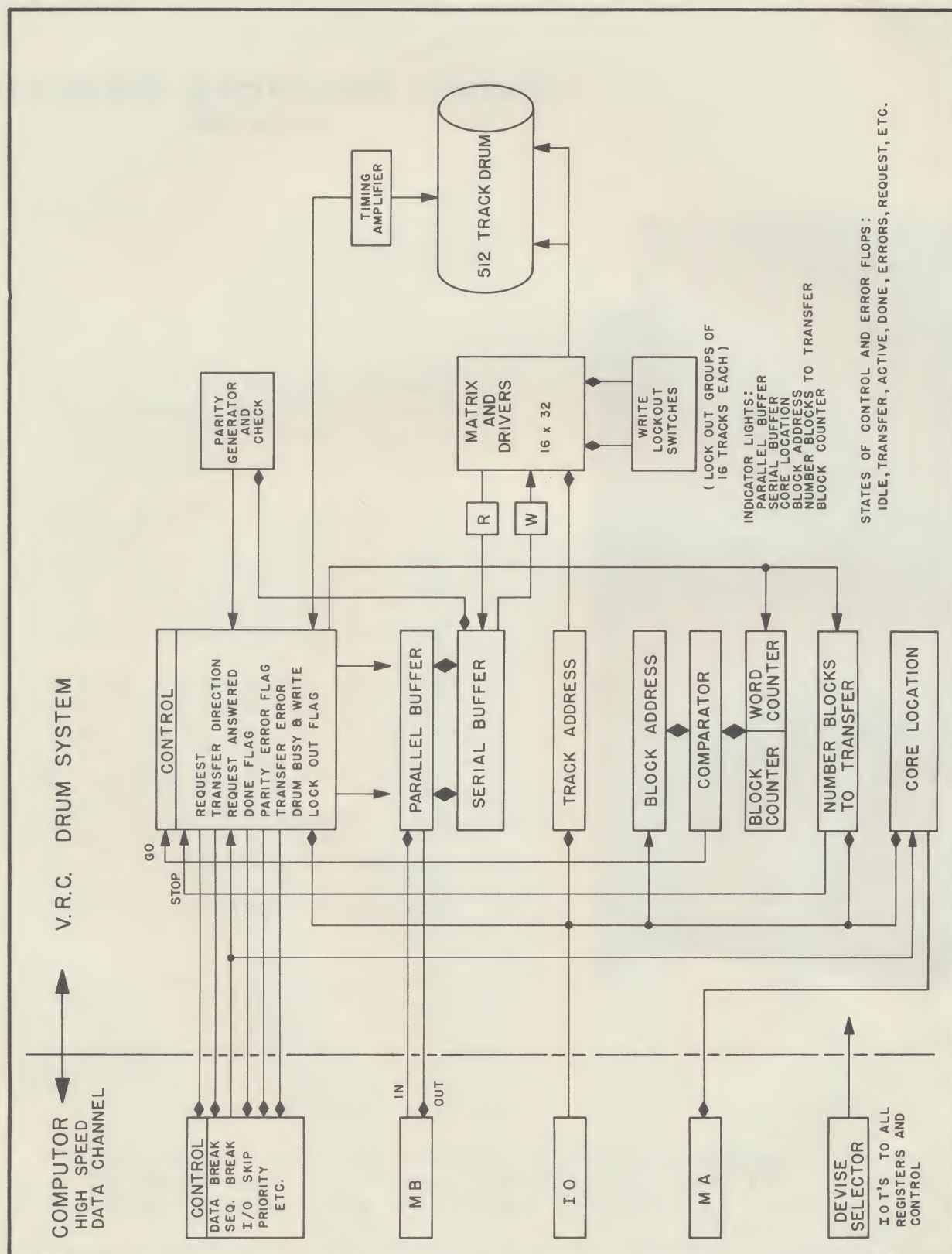
The VRC Type 1116 Serial Drum System is a peripheral data storage device for a high speed digital computer.

The System utilizes a standard VRC Model 1116B Magnetic Drum with a total storage capacity of 524,288 words of up to 24 bits in length on a maximum of 512 data tracks.

The drum can operate from a single phase source of either 50 or 60 cycles at an input voltage of 230 or 120 volts. At 60 cycles, the system can have drum speeds of either 1800 or 3600 RPM with a maximum access time of 34 or 17 milliseconds. At 50 cycles, the speed is reduced proportionally.

The complete system is mounted in a standard VRC cabinet with an external panel of indicator lights showing the state of the drum and internal logic.

A power supply and distribution within the drum system produce and control all operating voltages required. One source of external AC power is required, control of which may be exercised locally or remotely.



General:

The basic functions of the VRC Type 1116 Drum are data storage and retrieval, core memory address control, track and starting block address selection, blocks to be transferred, data request and transfer control, error checking, power supply and distribution. Two computer IOT instructions initialize the drum for a transfer. A single IOT instruction will transfer the next subsequent block of 64 words.

Write Mode:

Two IOT commands write 1 to 16 blocks of 64 words each. The first IOT clears the core location counter, loads the core location counter with the address of the first word to be written on the drum, sets the read/write flop to write and the HSC request flop, causing the computer to initiate a break cycle.

At the time of the break cycle, data is strobed into the parallel buffer and the HSC request flop is cleared. The second IOT clears and loads, from the IO register, the track address register, the starting block address register, and the number of blocks to be transferred register--and triggers a 40 μ sec delay to ensure sufficient time for track switching noise to settle. At the end of the delay period, the drum condition device (idle, transfer request (TRQ), run done) is set to the TRQ state. When the block counter equals the block address the condition device goes to run. At this time, the first word, which is in the parallel buffer, is transferred to the serial buffer and writing commences.

As each word is transferred from the parallel buffer to the serial buffer the request flop is set to a ONE, and the computer enters into a high speed channel break as previously described. If the previous request was not answered by the computer before the next word is demanded by the serial buffer (one word line) the transfer error flop is set to a ONE. This condition would indicate the same word was written in two subsequent drum word locations. As each ONE in the data word is written, a complementing flop is triggered, generating the odd parity bit, which is written just after the last data bit in each word. At the beginning of each word a blank or guard bit is written. This enhances the recording quality and also allows the necessary time for strobing data throughout the registers.

When the correct number of blocks has been written, as determined by the blocks to be transferred register, the drum condition device goes into the done state. At this time, the drum sends a done flag to the computer indicating that the drum has completed the transfer and is ready to accept another. The first IOT of the next initialization cycle will set the drum condition device to idle.

Read Mode:

Two IOT commands read 1 to 16 blocks of 64 words each. The first IOT clears the core location counter, loads it with the core address which will receive the first word read from the drum, and sets the read/write flop to read. The second IOT loads the IO register into the track address register, the starting block address register, and the number of blocks to be transferred register, and triggers a 40 μ sec delay which allows the track switching noise to settle. At the end of the delay period, the drum condition device is set to the transfer request state (TRQ).

When the block counter equals the block address, the condition device goes into the run state, the serial buffer is cleared and the data word starts shifting into the serial register. As each ONE in the serial buffer is shifted a parity flop is complemented, automatically checking for odd parity of ONES in the word. When the serial buffer is full, an overflow condition is created and the PB is cleared. Two drum clock pulses later, the contents of the serial buffer are strobed into the parallel buffer, the transfer error flop and parity error flop are sampled and the HSC request flop is set. When the computer completes its operating cycle it initiates a break cycle. At the time of the break cycle, the contents of the parallel buffer are strobed into the computer memory buffer and the request flop is cleared. When the correct number of blocks have been transferred, the drum goes into a done state as previously described.

Drum Condition:

The drum condition circuit is a four state device (Idle, TRQ, Run, Done) that controls the operation of the drum within a cycle. The condition device is connected so that once it attains a particular state it will stay there until an external action serves to change it.

When power is first applied to the drum, it is forced into the Idle state by the action of a power clear circuit which prevents the drum from being initialized until it is up to speed and the heads are flying. This is to prevent accidental erasure of recorded data by transients existing during power supply turn on. The action will be described later.

When the drum is initialized the second IOT starts a 40 μ sec delay as previously described. After this delay period if the drum is idle and not busy, the output of the TRQ gate will be pulled to ground thus forcing the drum into the TRQ state. The output of this gate conditions another gate so that when the block address equals the block counter and the guard flop goes to a ONE, the output of the second gate will condition a CD gate.

The next ϕA pulse will put the condition device into run. The output of the run gate is used as an enabling level in various parts of the system, such as the writer, the SB, etc.

When the drum has transferred the required number of blocks, as determined by the program, the blocks to be transferred counter issues a stop command and the drum goes into the done state. This causes a done flag and a sequence break pulse to be sent to the computer.

When the next IOT is sent, the drum will go into idle in preparation for the next transfer.

The busy state is coincident with either the TRQ state or the run state. If at any time during a transfer the computer tries to re-initialize the drum, a pulse is generated which sets the busy device to a ONE. This in turn causes a busy flag and a sequence break pulse to be sent to the computer notifying the programmer that he cannot gain access to the drum until the present transfer has been completed.

Address Decoding:

Y Track Address Decoding

The Y track address register is a VRC 2401 quad flop wired as a four bit counter. The outputs of the counter are wired through load driving inverters to the input gates of two VRC 2302 Y select packages. At the time of the second transfer IOT, the counter is cleared and the Y address of the desired track is loaded into the counter of the computer. Each time the drum index appears, if the drum is in the run state, the Y address is incremented by one. After 16 counts, the Y counter contains all ONES and the X address counter will be incremented by one. In this manner, all tracks will be sequentially addressed if the program contains a continued instruction.

X Track Address Decoding

The X address counter is identical to the Y counter with one additional flop which makes it a 32 bit counter. TXA and TXB connect directly to the decoding inputs of the VRC 2301 X select packages. TXC through TXE connect to the inputs of VRC 2504 positive diode gates for additional decoding.

Each of the 32 X select circuits has a SPST switch connected to one leg of the input AND gate which will connect the gate leg to ± 5 V when down, thus enabling the leg as long as it is in this position. If the switch is up, the leg will be connected to the read/write flop output placing a disabling ground level on the

leg if the flop is in the write condition. This action will keep the X select circuit from connecting the write to the magnetic head thus completely locking out 16 tracks.

If a programmer addresses a locked out track, he must be made aware of the fact. Each X select circuit has a sensing output that goes positive when the circuit is selected. Each one of these outputs is tied to an input gate leg of a VRC 2504 gate. The outputs of all these gates are ORed together and the common output will be at ground unless a locked out X select was addressed. If this happens, the gate output will go to ± 5 V causing a lock out flag as previously discussed.

Parallel Buffer (PB)

The parallel buffer is a clearset register that serves as an intermediate storage for data between the drum and computer. During the write mode the data word is loaded into the PB from the computer memory buffer via the set gate of each flop. In the read mode the contents of the serial buffer is loaded into the PB via the set gates with the common load lines. Associated with the PB are the memory buffer, in and out converters, and status light drivers.

Serial Buffer & Control (SB)

The SB and Control consists of the SB proper control and synchronizing circuits. The SB is a shift register with a parity generating flop associated with it. The control circuitry consists mainly of multi-legged AND gate to sense an overflow condition and an overflow shift register to synchronize the operation of the SB.

At the index time the SB, the overflow flop, the parity flop, and the WD flop are set to ZERO. The guard flop, the SBg flop, and the SBs flop are set to a ONE.

Drum Core Location Counter (DCL)

The DCL is a 16 bit flip-flop counter made up of four VRC 2401 guard FF packages. It is cleared and loaded with the computer core address at the time of each drum cycle by the first IOT. It is automatically incremented by one at the time of each HSC break cycle.

Associated with the DCL are the IO input converters, the MA output converters, and the status light drivers.

Status Light Drivers

The light drivers are standard VRC 2502 inverters that have the load driving capability to operate the various status lights on the system indicator panel.

System Timing - Figure 3

ϕA is the clock as directly derived from the track recorded on the drum. The width may be specified from 0.1 μsec to a maximum of 50% duty (approximately 0.4 μsec). Rise and fall will be less than 0.05 μsec when loaded with up to 10 ma in either direction.

ϕB is ϕA delayed by 1/2 a pulse period (within approximately $\pm 0.05 \mu\text{sec}$).

Write data is one side of an R-S-T flop. To write a ONE, ϕA will be gated with the data to set the flop. To write a ZERO, ϕA will gate with data to reset the flop. ϕB will always trigger the flop.

Write enable is a +5 V level active for the number of consecutive bit cells to be written. Write enable is gated with write data on one side of the writer and write enable and write data on the other side. Extra gate legs (total 4 each side) are available on the writer. (All signals are ZERO or disable at ground and a ONE or enable at +5 V).

Three outputs are available from the sense amplifier. The linear output is the output of the selected head amplified by a gain of approximately 60 (30 mv p-p to 1.8 V p-p typical). The level output is normally at ground until the linear signal swings more positive than the variable threshold (set at about ground with phase modulation recording). The output goes from +5 V to 0 when the threshold is exceeded. This level may be strobe gated (time sampled) externally to recover the information, if desired. It will drive 2 ma in either state. The output is normally at the pulse out which goes to +5 volts from ground when there is a coincidence of a positive signal at the linear out which exceeds the threshold and a read strobe which should be a 5 volt pulse with a rise time of less than 0.05 μsec . Pulse out will drive 10 ma in either state and may be preset to give output widths of 0.05 to 0.7 μsec . Read strobe is ϕA delayed about 0.6 μsec .

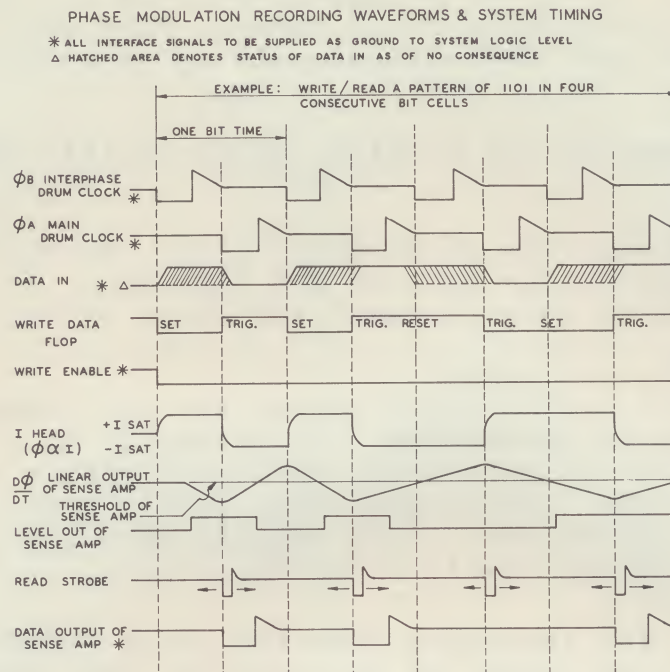


Figure 3

ABBREVIATIONS

IO	Input/Output Register
IOT	Input/Output Transfer
HSC	High Speed Channel
TRQ	Transfer Request
PB	Parallel Buffer
MA	Memory Address
SB	Serial Buffer
CD	Capacitor Diode Gate
WD	Write Data
DCL	Drum Core Location Counter
TXc-e	Track Address - X select C-E
TXa-b	Track Address - X select A-B
TYf-j	Track Address - Y select F-J

**Vermont Research
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AREA CODE 802
886-2256

February 16, 1967

T. Nelson
Box 1546
Poughkeepsie, New York

Attention: T. Nelson

Dear Mr. Nelson:

Enclosed is the information you asked for on Vermont Research Corporation Drum Memories. The actual specification is for a complete drum system ready to be incorporated with most computer high speed data channels.

The price of the complete system is approximately \$40,000. The drum with heads and read/write and track selection electronics sells for approximately \$20,000.

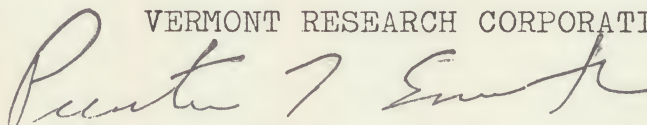
If you have further questions concerning this drum or smaller ones, we will be happy to send you our complete brochure covering 15 models in 3 series presently being manufactured by Vermont Research Corporation.

Prices for other drums range from \$1,000 to \$100,000 depending upon the size of the drum required and the specification for control circuits.

We would be pleased to furnish a complete proposal and quotation covering any of your Magnetic Drum Memory requirements.

Very truly yours,

VERMONT RESEARCH CORPORATION



Prentiss L. Smith
Vice President, Sales

PLS:e